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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/909,013	07/19/2001	Makoto Yoshino	TIJ-29448	8724

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EXAMINER	
GEYER, SCOTT B	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/909,013	YOSHINO ET AL.	
	Examiner	Art Unit	
	Scott B. Geyer	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-10,12,14,15 and 17-19* is/are rejected.

7)☒ Claim(s) *11,13 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The finality of the previous office action, mailed to the applicant on 4-8-2003, is withdrawn. A new non-final rejection of the pending claims (5-19) and a response to the applicant's arguments follows.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 8, 9, 10 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3A. As to **claim 8**, the examiner is confused as to the claim language of lines 4 and 5, specifically: "and a *for-plating-electricity-supply-use* conductor pattern electrically connected with the array of circuit patterns". As this section of the claim is not understood by the examiner, for purposes of examination, the examiner will interpret a "*for-plating-electricity-supply-use* conductor pattern" to be a "conductive pattern".

3B. As to **claim 9**, the examiner is confused as to the claim language of lines 8 through 11, specifically: "forming a *for-plating-electricity-supply-use* conductor pattern electrically connected with the plurality of circuit patterns". As this section of the claim is not understood by the examiner, for purposes of examination, the examiner will interpret a "*for-plating-electricity-supply-use* conductor pattern" to be a "conductive pattern".

3C. As to **claim 10**, the examiner is confused as to the claim language of lines 3 and 4, specifically: "using the *for-plating-electricity-supply-use* conductor pattern". As this section of the claim is not understood by the examiner, for purposes of examination, the examiner will interpret a "*for-plating-electricity-supply-use* conductor pattern" to be a "conductive pattern".

3D. As to **claim 12**, the examiner is confused as to the claim language of lines 4 and 5, specifically: "and a *for-plating-electricity-supply-use* conductor pattern electrically connected with the plurality of circuit patterns". As this section of the claim is not understood by the examiner, for purposes of examination, the examiner will interpret a "*for-plating-electricity-supply-use* conductor pattern" to be a "conductive pattern".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 5-10 and 12 are rejected under 35 U.S.C. 102(a) as being anticipated by Cho (6,235,555 B1).

5A. As to ***claim 5***, Cho teaches a method of forming an insulation film 68 which is a substrate for carrying a semiconductor chip 21, as seen in figure 9. The insulation film 68 has sprocket holes 71 formed at regular intervals along each side of the film, and thus have a pitch **L**. A two-dimensional array of through holes 62 are formed in

insulation film 71 between the sprocket holes, and adjacent through holes are spaced at regular intervals from each other as is clearly shown in figure 10B, and thus have a pitch **p** in relation to each other.

5B. As to ***claim 6***, Cho teach a sprocket holes and through holes spaced at regular intervals, which thus have pitches **L** and **p**. As neither **n**, **m**, **L** or **p** are defined in the claim, two integers **n** and **m**, where **n<m**, could satisfy the equation **(m*p)=(n*L)**.

5C. As to ***claim 7***, Cho teach sprocket holes 71 formed along both sides of the insulation film 68. The sprocket holes are used to advance the film along, in combination with toothed sprocket mechanism. As the film is advanced, through holes are formed in the film (column 4, line 22 et seq.). Neither **n** nor **L** are defined by applicant's claim - - the sprockets taught by Cho have a pitch **L** and they are moved a length **n*L** by the sprocket tooth mechanism.

5D. As to ***claim 8***, Cho teaches a two dimensional conductor pattern (as evidenced by the conductor wires as seen in figure 9). Cho also teaches a conductive plating connected with the conductor pattern (column 5, lines 1-7).

5E. As to ***claim 9***, Cho teaches a method of forming an insulation film 68 which is a substrate for carrying a semiconductor chip 21, as seen in figure 9. The insulation film 68 has sprocket holes 71 formed at regular intervals along each side of the film, and thus have a pitch **L**. A two-dimensional array of through holes 62 are formed in insulation film 71 between the sprocket holes, and adjacent through holes are spaced at regular intervals from each other as is clearly shown in figure 10B, and thus have a pitch **p** in relation to each other. Cho also teaches a chip mounted to the insulation film

and electrically connected to the conductive patterns of the insulation film, encapsulation of the mounted chip and separation of the insulation film into individual packages (see figure 13, numerals 92-95).

5F. As to ***claim 10***, Cho teaches plating of gold upon a layer of copper to make the conductive patterns (column 4, lines 66-67, continued to column 5, lines 1-7).

5G. As to ***claim 12***, Cho teaches a two dimensional conductor pattern (as evidenced by the conductor wires as seen in figure 9). Cho also teaches a conductive plating connected with the conductor pattern (column 5, lines 1-7).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 14, 15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (6,235,555 B1) in view of Hayashi et al. (6,192,579 B1).

7A. As to ***claim 14***, Cho teaches a method of packaging a semiconductor device, wherein an insulation film 68 is a substrate for carrying a semiconductor chip 21, as seen in figure 9. The insulation film 68 has sprocket holes 71 formed at regular intervals along each side of the film, and thus have a pitch **L**. A two-dimensional array of through holes 62 are formed in insulation film 71 between the sprocket holes, and adjacent through holes are spaced at regular intervals from each other as is clearly

shown in figure 10B, and thus have a pitch **p** in relation to each other. Cho also teaches mounting a semiconductor chip on the insulation film, encapsulating the chip in sealing resin and separating the film into individual resin coated chip packages (see column 6, lines 33-49). Cho does not teach mounting a chip directly *over* the through holes. However, Hayashi et al. teach mounting a chip on an insulation film directly over through holes in the film, as shown by figures 5 and 8. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method of Cho with the mounting method of Hayashi et al. so as to reduce the overall size of the individual package (i.e., reduce the footprint of the package).

7B. As to ***claim 15***, Cho teaches an insulation film 68 as a substrate for carrying a semiconductor chip 21, as seen in figure 9. The insulation film 68 has sprocket holes 71 formed at regular intervals along each side of the film, and thus have a pitch **L**. A two-dimensional array of through holes 62 are formed in insulation film 71 between the sprocket holes, and adjacent through holes are spaced at regular intervals from each other as is clearly shown in figure 10B, and thus have a pitch **p** in relation to each other. Further, the through holes are arranged in relation to each other in an array and are formed continuously along and across the film and within the circuit regions.

7C. As to ***claim 17***, Cho teaches an insulation film 68 as a substrate for carrying a semiconductor chip 21, as seen in figure 9. The insulation film 68 has sprocket holes 71 formed at regular intervals along each side of the film, and thus have a pitch **L**. A two-dimensional array of through holes 62 are formed in insulation film 71 between the sprocket holes, and adjacent through holes are spaced at regular intervals from each

other as is clearly shown in figure 10B, and thus have a pitch **p** in relation to each other. Further, the through holes are arranged in relation to each other in an array and are formed continuously along and across the film.

7D. As to ***claims 18 and 19***, Hayashi et al. teach formation of metal solder in the through holes (see column 6, lines 1-5).

Allowable Subject Matter

8. Claims 11, 13 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 11, 13 and 16, which depend on independent claim 9 and 10 respectively, teach a dicing step wherein the dicing blade has a blade trim width which is wider than the wiring width of the 'sub-line' of the conductor pattern and the 'sub-line' is not left behind on the insulation film after the dicing step has been performed. The cited prior art does not teach dicing using a dicing blade having a blade width wider than the wiring width of the 'sub-line'.

Response to Arguments

9. Applicant's arguments filed 9-11-03 within the appeal brief have been fully considered. The applicant's contention on page 4 is that the applicant's admitted prior art teaches multiple through holes but not a "two-dimensional array" of through holes, and the applicant has also provided a dictionary definition of the meaning of 'array'. The above rejections have been modified to provide references which are consistent with

the applicant's view of an 'array', meaning an arrangement of quantities, in this case through holes, in a rectangular row and column format. The above cited references of **Cho** and **Hayashi et al.** both teach an 'array' of through holes, which can be plainly seen by their accompanying figures, as cited. Since an array, by the applicant's provided definition has rectangular quantities of rows and columns, then the examiner interprets that the through holes in an insulation film must then be in some sort of geometric pattern, instead of for example randomly punched into the film. Therefore, the through holes of the references satisfy the definition provided by the applicant. For example, in the reference of Cho, figure 9, (on the upper left hand side of the figure), there exists two arrays of through holes within the chip mounting area, wherein each array has 4 through holes arranged in 1 row and 4 columns (or 4 rows and 1 column, depending upon how the figure is viewed).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer whose telephone number is (571) 272-1958. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. E-mail: scott.geyer@uspto.gov

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SBG
February 9, 2004

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